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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/661,203	SHIVJI ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) 1,2,4,5,8-10,12,13 and 16-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4,5,8-10,12,13 and 16-22 is/are rejected.

7)☒ Claim(s) 23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. An objection to the drawings is withdrawn since it is being amended accordingly.
2. Claims 1,2,4,5,8-10, 12,13,and 16-22 are rejected by the new ground(s) of rejection necessitated by the amendment.

Claim Objections

3. **Claim 9** is objected to because of the following informalities. Appropriate correction is required.

   Claim 9 recites, "...**means for transmitting the SONET/SDH formatted data ; at the cross-connect card; ...**"in line 8-12. The use of semicolon ";" between these two limitation makes the claim unclear. Thus, it should be removed or revised.

4. **Claim 23** objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

   Claim 23 recites, "...**the first ASIC** is configured to..." in line 2 and "...**the second ASIC** is configured to ..." in line 5, which further limit the each functionally of ASIC within the cross-connect card. The independent claim 17 (i.e. a previous claim) does **not** even recite that a cross connect card includes a first and second ASIC. However, it is noted that claim 22 recites, a cross connect card includes a first and second ASIC.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2,4,5,8-10,12,13,16,17, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Upp (U.S. 4,967,405).

Regarding Claims 1 and 9, Upp'405 discloses an apparatus **(see FIG. 1, Digital Cross connect System 10)** to perform a method comprising:

means for receiving network data in a first format **(see FIG. 1, DS-0, T1, or CEPT signal format)** via a first card **(see FIG. a combined system of ADM, 700a -700d, and SBI interface module/card; see FIG. 6-7)** coupled to a first network **(see FIG. 1, the low speed/asynchronous network that couples to each ADM card; see col. 2, lines 55-57; col. 7, lines 25-40)**;

means for converting the data to a synchronous optical network (SONET/SDH) format **(see col. 2, lines 58-60; the received signal/data are converted into SONET formatted signal)**;

means for transmitting the SONET/SDH formatted data as one or more serial data signals **(see FIG. 1, SBI 600 produces/transmits a serial/multiplexed SONET formatted data/signals from ADM cards 700a-700d ; see col. 7, lines 17-20)** to a cross-connect card **(see FIG. 1, a combined system of VTX 900 and WBX 800; see col. 7, lines 41-63)** via a backplane **(see FIG. 1, a combined system of data buses which connect the**

cards/modules (i.e. modules 700a-d, SBI 600, VTX 900, DS3A 1200, WBX 800, SPT 400, 21M 300, Mux 200, Line interfaces 100), thus, it is clear that the combined system of data buses in the modular system is a backplane; see col. 4, lines 10-14);

means for performing switching functions on the SONET/SDH formatted data at the cross-connect card (**see col. 7, lines 41-63; note that SONET formatted data (i.e. VTs and STSs) are switched in the combined system of VTX and WBX cross-connect**);

means for transmitting the SONET/SDH formatted data; at the cross-connect card (**see col. 3, lines 15-20, see col. 4, lines 33-45; note that SONET formatted data are transmitted at the combined system of VTX and WBX, and they are cross-connected via non-blocking switching**);

means for transmitting the SONET/SDH formatted data as one or more serial data signals to a second card (**see FIG. 1, a combined system of 31M 300a, Scrambler Mux 200 and SONET line interface 100; see col. 6, lines 27-48; note that multiplexed/serial SONET STS-1/ STS-3 data is transmitted toward the combined system of 31M 300a, Scrambler Mux 200 and SONET line interface 100**) coupled to a second network (**see FIG. 1, the second/optical high-speed network that couples to line interface unit 100; see col. 6, lines 19-27**);

means for converting the SONET/SDH formatted data to a second format (**see FIG. 1, OC-24/STS-24 format; see FIG. 2a-b; see col. 8, lines 19-29; SONET/SDH STS-1/STS-3 data are converted/multiplexed into STS-24/OC-24 format (or two STS-12)**);

means for transmitting the data in the second format to the second network via the second card (**see FIG. 1, OC-24/STS-24 format signal is transmitted toward the**

second/optical high-speed network that couples to line interface unit 100; see col. 6, lines 18-27, see col. 2, lines 32-36).

Regarding Claim 17, Upp'405 discloses a system (**see FIG. 1, Digital Cross connect System 10**) comprising:

a first card (**see FIG. 1, a combined system of ADM, 700a -700d, and SBI interface 600 module/card, and FIG. 6-7**) coupled to a first network (**see FIG. 1, the low speed/asynchronous network that couples to each ADM module; see col. 2, lines 55-57; col. 7, lines 25-40**) compatible with a first data format (**see FIG. 1, DS-0, T1, or CEPT signal format is compatible/match with its corresponding ADM module**), the first card being configured to convert data from the first data format to a synchronous optical network (SONET/SDH) format (**see FIG. 7, SONET STS and VT format**) and vice versa (**see col. 2, lines 58-60; the received DS-0, T1, or CEPT signal/data are converted to/from SONET formatted signal**);

a second card (**see FIG. 1, a combined system of 31M 300a, Scrambler Mux 200 and SONET line interface 100, and FIG. 2-3**) coupled to a second network (**see FIG. 1, the second/optical high-speed network that couples to line interface unit 100; see col. 6, lines 19-27**) compatible with a second data format (**see FIG. 1, OC-24/STS-24 (i.e. two STS-12) format is compatible/matched with its corresponding the combined system of 31M 300a, Scrambler Mux 200 and SONET line interface 100 module**), the second card being configured to convert data in the second data format to the SONET/SDH format, and

vice versa (**see FIG. 2a-b; see col. 8, lines 19-29; SONET/SDH STS-1/STS-3 data are converted/multiplexed/de-multiplexed to/form STS-24/OC-24 format (or two STS-12)**);

a cross-connect card (**see FIG. 1, a combined system of VTX 900 and WBX 800; and FIG. 8-9; col. 7, lines 41-63)** configured to perform switching functions on data in the SONET/SDH format (**see col. 7, lines 41-63; note that SONET formatted data (i.e. VTs and STSs) are switched in the combined system VTX and WBX cross-connect**); and

a backplane (**see FIG. 1, a combined system of data buses in the system 10)** communicatively connecting the first card, second card, and cross-connect card, (**see FIG. 1, a combined system of data buses which connect the cards/modules (i.e. modules 700a-d, SBI 600, VTX 900, DS3A 1200, WBX 800, SPT 400, 21M 300, Mux 200, Line interfaces 100), thus, it is clear that the combined system of data buses in the modular system is a backplane; see col. 4, lines 10-14**); the backplane being configured to carry data in the SONET/SDH format as one or more serial data signals between the first card, the cross-connect card, and the second card (**see col. 7, lines 17-20, see col. 6, lines 27-48; note that a combined system of buses is designed/configured to transmit a serial/multiplexed SONET formatted data/signals between the modules/cards in the system 10.)**

Regarding Claims 2 and 10, Upp'405 discloses wherein performing switching functions on the SONET/SDH formatted data comprises performing time switching and space switching (**see col. 7, lines 41-44, 56-62; note that the combined system of VTX and WBX switches the SONET formatted signal in space and time**.)

Regarding Claims 4 and 12, Upp'405 discloses wherein the one or more serial data signals are transmitted via the backplane as a differential pair (see FIG. 2a-, four STS-3 inputs 210a-210d and a spare STS-3 input 210e; **see col. 8, lines 19-44; note that each serial/multiplexed STS-3 signal is transmitted through the combined system of the buses (i.e. backplane) in different/differential pair**.)

Regarding Claims 5 and 13, Upp'405 discloses wherein the data in the second format comprises an aggregation of multiple data signals in the first format (**see FIG. 2a-1, STS-3 inputs 210a-210e and col. 8, lines 19-45; see FIG. 3a, STS-1 inputs 310a-310c and col. 9, lines 64 to col. 10, lines 14; see FIG. 7, VTSPE 745a-b and T1/DS-1 inputs 728a-b, 738a-b and col. 14, lines 12-67; note that high speed STS-24/OC-24 (i.e. two STS-12/OC-12) comprises the multiplexed low speed signals (i.e. T1/DS1). Each DS1 signal is encapsulated into VT1.5 container and then multiplexed into the VTSPE, STS-1, STS-3, STS-12, and STS-24/OC-24, respectively.)**

Regarding Claims 8 and 16, Upp'405 discloses wherein the SONET/SDH formatted data according to **one** of STS-1, STS-3, STS-12, STS-48 and STS-192 protocols (**see FIG. 2a-1, STS-3 format protocol and col. 8, lines 19-45).**

Regarding claim 21,Upp'405 further teaches wherein the cross-connect card (**see FIG. 8a, the combined system of WBX 800 and VTX 900**) includes an application specific integrated circuit (ASIC) (**see col. 15, lines 35-51; WBX includes an application specific**

(i.e. CMOS) integrated circuit) configured to perform the switching functions on the data in the SONET/SDH format **(see col. 7, lines 41-63; note that SONET formatted data (i.e. VTs and STSs) are switched in the combined system of VTX and WBX cross-connect)**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 18-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Upp'405 in view of well-established teaching in art.

Regarding claim 18, Upp'405 discloses wherein the second card each include an application specific integrated circuit **(see col. 6, line 19-23; note that SONET line interface unit 100 is the SONET application specific integrated circuit)**, and both first and second cards configured to perform parallel-to-serial conversion and serial-to-parallel conversion on data in the SONET/SDH format **(see FIG. 1, a combined system of 31M 300a, Scrambler Mux 200 and SONET line interface 100 performs parallel-to-serial conversion (i.e. multiplexing) and serial-to-parallel conversion (i.e. demultiplexing) on SONET formatted data; also see multiplexing/de-multiplexing at FIG. 2a-1, STS-3 inputs 210a-210e and col. 8, lines 19-45; see FIG. 3a, STS-1 inputs 310a-310c and col. 9, lines 64 to col. 10, lines 14. Also, each combined system of ADM and SBI card/module (i.e. first card) also performs multiplexing/demultiplexing of SONET data format; FIG.**

7, VTSPE 745a-b and T1/DS-1 inputs 728a-b, 738a-b and col. 14, lines 12-67; see FIG. 6).

Upp'405 does not explicitly disclose wherein the first card includes an application specific integrated circuit (ASIC).

However, the above-mentioned claimed limitations are taught by well-established teaching in art. In particular, well-established teaching in art teaches wherein the first and second cards each include an application specific integrated circuit (ASIC). **It is well known in the art that, the circuit packs are implemented with ASIC. In particular, Upp'405's ADM module (see FIG. 7) already contains digital circuitry, and it can further include/modify with an ASIC with SONET/T-carrier specific intergraded circuit similar to high-speed circuit packs/modules.**

In view of this, having the system of Upp'405 and then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Upp'405, by providing an ASIC on first/T3 low speed interface card/module, as taught by well established teaching in art. The motivation to combine is to obtain the advantages/benefits taught by well established teaching in art since well established teaching in art states that such modification would provide smaller, lighter and economical card/module/circuit pack by utilizing the intergraded circuit or chip technology.

Regarding claim 19, the combined system of Upp'405 and well-established teaching in art discloses all aspects of the claimed invention set forth in the rejection of Claim 17 and 18 as described above, in particular including ASIC on each interface card/module.

Upp'405 further teaches wherein perform parallel-to-serial conversion on the data in the SONET/SDH format (**see FIG. 1, SBI 600 produces/transmits a serial/multiplexed SONET formatted data/signals from parallel ADM cards 700a-700d ; see col. 7, lines 17-20**), thereby making the data suitable for transmission to the cross-connect card via the backplane (**FIG. 7, VTSPE 745a-b and T1/DS-1 inputs 728a-b, 738a-b and col. 14, lines 12-67; see FIG. 6; note that SONET VT signals must be multiplexed in order to transmit towards the VTX 900 via the bus for switching**). Thus, it is clear that ASIC on each interface card/module can be programmed/designed to perform above-mentioned steps.

Regarding claim 20, the combined system of Upp'405 and well-established teaching in art discloses all aspects of the claimed invention set forth in the rejection of Claim 17 and 18 as described above, in particular including ASIC on each interface card/module.

Upp'405 further teaches wherein perform serial-to-parallel conversion on the data in the SONET/SDH format (**see FIG. 1, SBI 600 receives a serial SONET formatted data/signals and transmits a parallel/de-multiplexed toward ADM cards 700a-700d; see col. 7, lines 17-20**), the data being received from the cross-connect card via the backplane (**FIG. 7, VTSPE 745a-b and T1/DS-1 inputs 728a-b, 738a-b and col. 14, lines 12-67; see FIG. 6; note that SONET VT signals received via the bus from the VTX 900 must be de-multiplexed in order to transmit towards ADM modules/cards**). Thus, it is clear that

ASIC on each interface card/module can be programmed/designed to perform above-mentioned steps.

Regarding claim 22, Upp'405 further teaches wherein the cross-connect card includes a first circuit (**see FIG. 1, VTX, 900**) and second application specific integrated circuit (ASIC) (**col. 15, lines 35-51; WBX includes a application specific (i.e. CMOS) integrated circuit)**, each of the first and second circuit being configured to perform parallel-to-serial conversion (**see FIG. 1, VTX 900 is designed/configured to receive parallel inputs from SBI 600 and transmitted into a serial output towards WBX 900 in SONET format; Similarly, WBX 900 is designed/configured to receive the parallel inputs from SPT 400 (i.e. STS-1) and transmitted a serial output towards VTX in SONET format)** and serial-to-parallel conversion on data in the SONET/SDH format (**see FIG. 1, VTX 900 is designed/configured to receive a serial input from WBX and transmitted into the parallel outputs toward SBI 600 in SONET format; Similarly, WBX 900 is designed/configured to receive a serial input from VTX and transmitted the parallel outputs toward SPT 400 (i.e. STS-1) in SONET format)**.

Upp'405 does not explicitly disclose wherein the first circuit includes an application specific integrated circuit (ASIC).

However, the above-mentioned claimed limitations are taught by well-established teaching in art. In particular, well-established teaching in art teaches wherein the first circuit includes an application specific integrated circuit (ASIC). **It is well known in the art that, the circuit packs/modules are implemented with ASIC. Upp'405's VTX module (see**

FIG. 9a-c) already contains digital circuitry, and thus it can further include/modifies an ASIC with application (i.e. CMOS) integrated circuit as WBX module, as per well established teaching in art.

In view of this, having the system of Upp'405 and then given the teaching of well established teaching in art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Upp'405, by providing an ASIC on for VTX card/module, as taught by well established teaching in art for the same motivation as described above in claim 18.

Allowable Subject Matter

7. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1,2,4,5,8-10,12,13 and 16-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 703-305-4798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
5/3/04

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PRIMARY EXAMINER